How Many ADC Counts in One MIP?

Vince's estimation of MIP peak is confusing. On slide 6 it is 67, but on slide 8 he position it at 35. See
http://www.phenix.bnl.gov/cdsagenda//askArchive.php?base=agenda&categ=a08225&id=a08225s1t1/moreinfo

We measured (with Rachid on 03/27) the calibration pulse position at 75 ADC counts above pedestal.
The injected charge = Vvcal*Cf, Where Cf = 25fF. Where Vvcal is the voltage on the VCAL line. The schematic for setting the Vvcal is as follows:

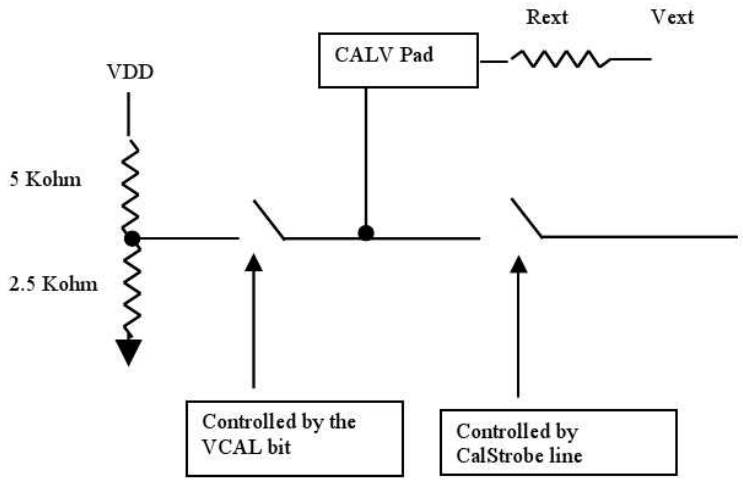


Figure 12 Cartoon schematic for the Vcal circuit in the SVX4 chip.

We set VCAL parameter to 1. Not sure how Vext applied to SVX4s in ROC3. The best way would be to measure the VCAL directly on connector (J1.49 and J2.49, Rext = 1K). Assuming that Vext was disconnected then Vvcal = 0.8V and injected charge is 21 fC.

The MIP particle will deposit 7fC in 0.6mm silicon.

If all our assumption correct then the calibration pulse correspond to 3 MIP, and one MIP correspond to 25 ADC counts. Large discrepancy with Vince's 67 ADC counts.

We also should take into account that the MIP signal will be divided between X and Y strips, so it will be even less ADC counts per 1 MIP in one strip.

To check:

1) Voltage on Vext.
2) How optimal is CALStrobe relative to FEClk.

Contribution to noise from the leakage current is negligible.

This is response to Rachid's argument.
The RMS of the shot noise measured by charge sensitive amplifier over time interval **t** is **RMSshot = sqrt(eIt)**. Where **e** is electron charge, **I** is the leakage current. Assuming t=75ns, and I=1nA, then RMSshot = 3.4e-18 C, (**yes it is only 20 electrons)**, and it is negligible.

Expected noise of SVX4

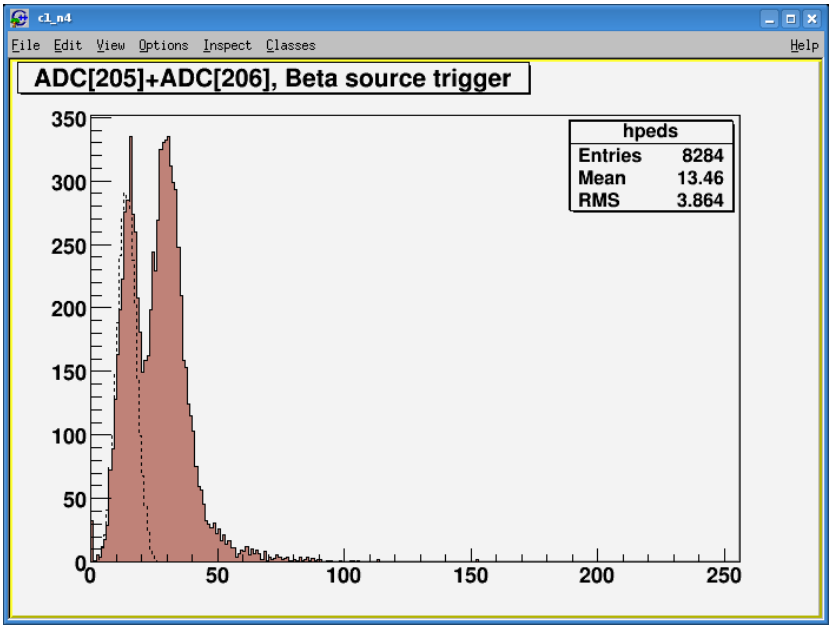
The manual claims for 2000e for 40pF and 100ns integration. This correspond to 0.3fC or 1 ADC count in our calibration scheme.

The report
http://www.phenix.bnl.gov/~suhanov/ncc/svx4/Note-SVX4-Results2.pdf
describes the noise performance of the SVX4. Interesting that an intermediate setting of the risetime results in less noise for larger capacitance.

Comparison with NCC strips

See: http://www.phenix.bnl.gov/~suhanov/ncc/tests/beta_source_test.pdf

NCC strip sensors are 60x60x0.3mm with 0.5mm strips. The capacitance ~6 pF.



Sum of amplitudes from two adjacent strips for events with selected trigger clock phases (2,3 and 4). The dashed line – from the pedestal run. The MIP peak is clearly seen.

The RMS of pedestals were of the order of 2-3 ADC counts. And the MIP peak

position is consistent with the calibration pulse as it is shown on the lower left graph of fig. 3.

Bias Scan

We made with Rachid the quick measurements with different bias setting and we did not see the difference in the pedestal widths and in position of calibration pulse. If that is correct then the noise we see is not related to the detector.
The bias scan for NCC strip sensors was measured last December and it is shown at:
http://www.phenix.bnl.gov/~suhanov/ncc/tests/beta_source_work/bias_scan.odt
The signal significantly grows, pedestals are slightly narrows for bias voltages between 10 to 20 volts. Above 20 V the signals and pedestals does not change much.
The same behavior should be with VTX sensors.

Effect of RTPS-real time pedestal suppression on pedestal width

We did not notice the difference in pedestal width when RTPS was on or off. That means that contribution of common mode noise or low frequency EM pick-up is negligible.

Suggestions for the noise management plan

1. Start with sensor not attached. Or at least check the wires which are not wire bonded. The rms noise should be less than 0.5 fC. If it is higher – check for the shape of the pedestals line is it changing from event to event?
2. With sensor disconnected – check the pedestals when all channels are disabled.
3. Optimize position of the CALStrobe relative to FEClk.
4. Are the preamp risetime and FEClk duty cycle optimal?
5. Is Rref_sel position optimal? See page 19 of SVX4 description.
6. Try to increase/decrease clock frequency, i.e. double it. Expect narrower/wider (sqrt(2) times) pedestals and completely different shape of the pedestal line (if the significant noise contribution comes from a high frequency pick-up.
7. With sensor attached, check for pedestals when all channels disabled. The rms noise should be less than 0.5 fC.
8. With sensor attached, check the channels with disconnected wires, they should have rms noise less than 0.5 fC. Similarly, the channels with touching wires should show increased noise.
9. Make bias scan and measure amplitude of the calibration pulse and the width of the pedestals. It should change for low bias settings!